Keyboard Encoder Circuits

MM5745, MM5746 78-key keyboard encoder

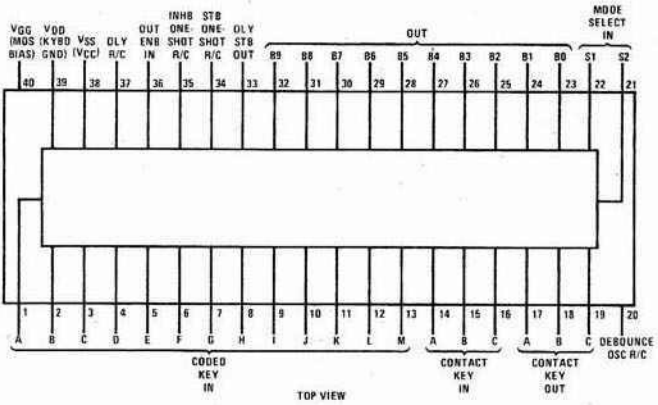
general description

The MM5745, MM5746 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 78 double-pole single-throw switches (hall-effect, capacitive, or contact) into a 10-bit code. Full quad-mode operation allows 4 independent 10-bit codes per switch. Debounce circuits for contact keys are provided for 3 function switches. The MM5745, MM5746 is fabricated with low threshold metal gate P-channel enhancement devices and ion-implanted resistors and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

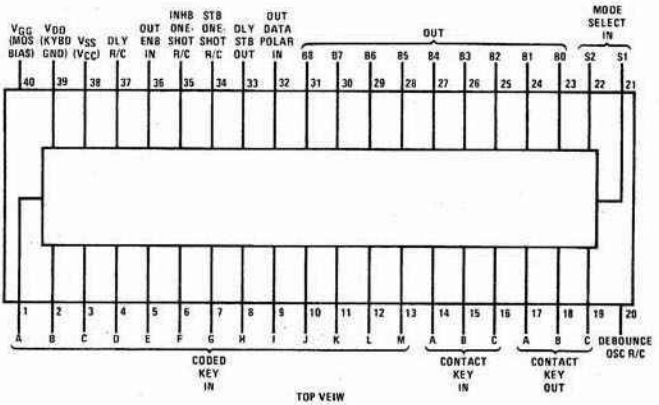
features

- 78- key quad-mode capability
- N-key/2-key rollover
- 1 character data storage
- Level or pulse data strobe output
- Data strobe pulse width control
- Key bounce delay control
- Function key debounce circuits
- Data and Strobe outputs directly compatible with TTL/DTL or MOS logic

connection diagrams (Dual-In-Line Packages)



Order Number MM5745N
See Package 24



Order Number MM5746N
See Package 24

absolute maximum ratings

Voltage at Any Pin Except Outputs	V_{SS} + 0.3V to V_{SS} − 25V
Voltage at Any Output Pin	V_{SS} + 0.3V to V_{SS} − 20V
Power Dissipation	700 mW at T_A = 25°C
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	With Respect to V_{SS}			−1.5	V
V_{IL}	Low Level Input Voltage	With Respect to V_{DD}			0.8	V
V_{OH}	High Level Output Voltage	With Respect to V_{SS}			−1.8	V
V_{OL}	Low Level Output Voltage	With Respect to V_{DD}, I_{OL} = 1.6 mA			0.4	V
I_{IL}	Low Level Input Current (Logic)	V_{SS} = 5.25V, V_{IN} = 0.4V (Not Including MOS Inputs), (Note 2)			−1.6	mA
t_r	10–90% Output Rise Time	C_L = 50 pF			1	μs
t_f	90–10% Output Fall Time	C_L = 50 pF			1	μs
t_d	Delay Time Input to Output	Delay Capacitor = 0, R_L = 200Ω			20	μs
t_s	Delay from Strobe to Data Output		0.5			μs
D_{td}	Delay R/C Time Delay	±25% Variation Max per Given Set of R and C	40		80	μs
		R–Useful Range	200		680	kΩ
		C–Useful Range at Min R	0.001		0.002	μFd
I_{td}	Inhibit One-Shot Time Delay	±25% Variation Max per Given Set of R and C	1		30	ms
		R–Useful Range	200		680	kΩ
		C–Useful Range at Min R	0.025		0.75	μFd
S_{td}	Strobe One-Shot Time Delay	±25% Variation Max per Given Set of R and C Typ	40		80	μs
		R–Useful Range	200		680	kΩ
		C–Useful Range at Min R	0.001		0.002	μFd
B_{td}	Debounce Oscillator	±25% Variation Max per Given Set of R and C	1		7	ms
		R–Useful Range	200		680	kΩ
		C–Useful Range at Min R	0.025		0.175	μFd
I_{SS}	Supply Current	V_{SS} = 5.25V			100	mA
I_{GG}	Bias Current	V_{GG} = −18V			5	mA

Note 1: V_{SS} = 5V ±5%, V_{DD} = Gnd, V_{SS} = −12V to −18V and T_A = 0°C to +70°C.
Note 2: The following inputs have internal pull-up resistors to V_{SS}: Output Enable, Output Data Polarity.

functional description

A block diagram of the MM5745 and MM5746 keyboard encoders is shown in *Figure 1*. Connection diagrams for these devices are shown on the previous page. The following discussions are based on *Figure 1*.

Coded Key Inputs

Thirteen MOS type coded key inputs, designated A–M can be coded in an M of N format. These codes must be specified with each reprogramming of the coding mask. A maximum of 78 input codes may be specified. Typically, coding takes the form of 2 out of 13 inputs.

Contact Key Inputs

Three MOS type contact key inputs designated A, B and C can be used to debounce contact type switches.

functional description (Continued)

Mode Select Inputs

Two mode inputs, designated S1 and S2, are used to select any 1 of the 4 output coding modes. The binary number selections to represent a given output code mode must be specified with each reprogramming of the coding mask.

Output Data Polarity Input (MM5746 Only)

The Output Data Polarity Input, when switched from one state to the other, causes a reversal of the output data polarity. When open, the input is held high, logical "1", by an internal pull-up resistor, and the data comes through non-inverted from the output ROM.

Output Enable Input

The Output Enable Input enables the output storage latches to accept new output data and allows an output strobe to be generated. When the input is open, an internal pull-up resistor holds the input high, logical "1", and enables the output. When held low, logical "0", the output and strobe are disabled.

Debounce Oscillator R/C Input

The Debounce Oscillator R/C Input is a timing input that can eliminate closing or opening contact bounce durations of between 1 to 2 clock periods. Depending upon the length of bounce and R/C values chosen, the output will be delayed from the inputs from 1 to 14 ms. The resistor connects to V_{GG} and the Capacitor connects to V_{SS}.

Strobe One-Shot R/C Input

The Strobe One-Shot R/C Input is a timing input used to adjust the width of the delayed output strobe. The strobe width has a ±25% variation for a given set of R and C. The pulse width range can be varied between 1 μs and 10 ms. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C input.

Inhibit One-Shot R/C Input

The Inhibit One-Shot R/C Input is a timing input used to disable the Encoder Chip outputs for a period of time after new data has appeared at the outputs and a strobe issued. The inhibit time is necessary to allow the Coded Key inputs to settle out after a keyswitch is depressed. The time slot is adjustable from 1–10 ms ±25%. The recovery time is less than 100 μs. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C Input.

Delay R/C Input

The Delay R/C Input is a timing input used to determine that valid data is present at the Coded Key Inputs. Valid data must be present continuously for some period of time adjustable between 40 and 80 μs ±25% before the data is accepted as valid data. The resistor and capacitor timing elements are connected as stated for the Debounce Oscillator R/C Input.

Contact Key Outputs

Three contact key outputs designated A–C provide bounce-free non-inverted outputs corresponding to their respective inputs.

Data Outputs

Ten Data Output lines designated B0–B9 are provided. The specific output code related to a given input code and mode must be specified with each reprogramming of the coding mask.

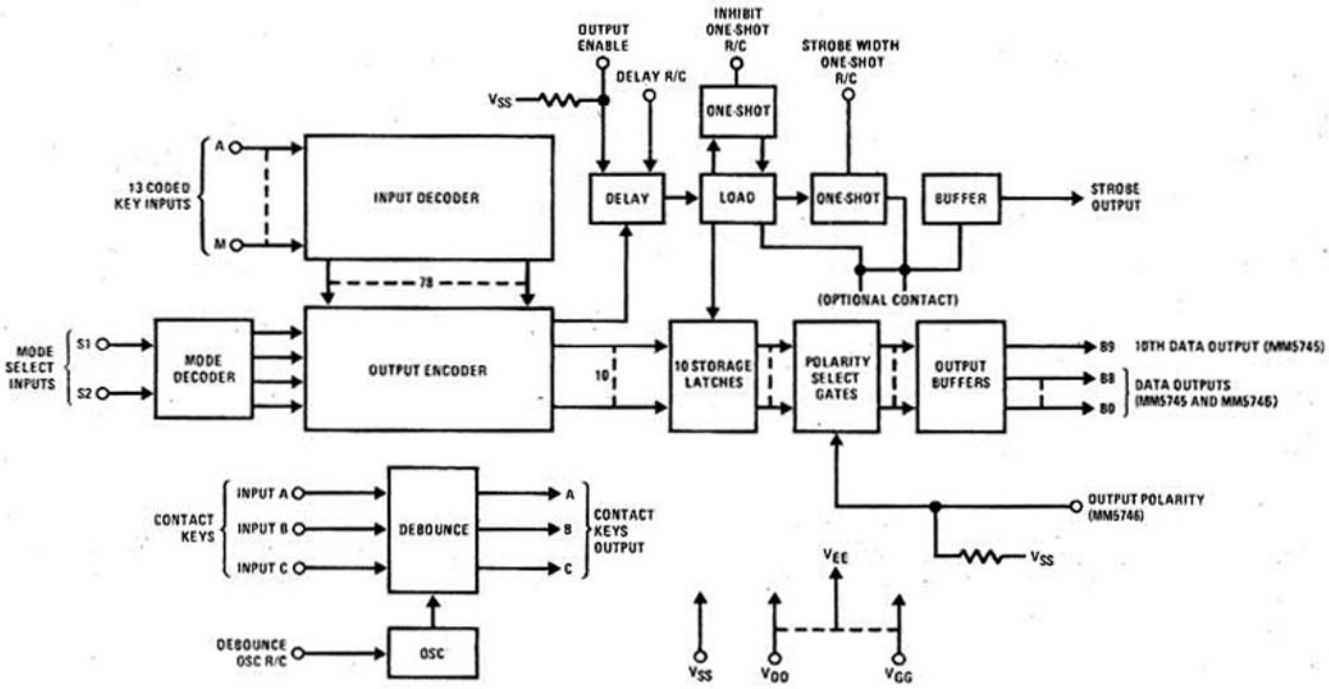


FIGURE 1

functional description (Continued)

Strobe Output

The Strobe Output is used to indicate that new data has just been placed on the Data Output lines.

Data Transfer

Input data, typically in a 2 out of 13 format, is introduced by depressing a keyswitch. The data passes through the input buffers, input inverters, and is decoded into single line codes if the data is valid. There are a maximum of 78 single line codes and these are coded into 41-bit output words. The 41st bit is used to enable the delay R/C timer. Valid input data must be present continuously for typically 60 μs before it is accepted as valid input data and the proper output codes and strobe are generated.

The status of the mode select inputs determines which of the 4 10-bit output codes are selected (first 40 bits). The mode select lines are programmable in binary format and therefore are decoded into single line codes. The output encode in reality has 82 input lines (78 input codes and 4 modes). When a valid input code is present and the mode is selected, the proper 10-bit word is steered through the Mode "OR" Gates and to the inputs of the storage latches. When the proper delay interval has elapsed, the load logic loads the new data into the storage latches.

Both polarities of the 10 data bits are fed to the Polarity Select Gates where the output Data Polarity Input selects the desired polarity output. The selected 10 data bits output the chip through the Output Buffers.

Logic Sequence

The Logic Sequence is not initiated until the successful completion of the delay timing cycle. At the completion of the delay cycle, 3 things happen almost simultaneously. First, a load signal of approximately 2 μs is fed to the storage latches to accept new data. Second, the Strobe Pulse, typically 60 μs wide, is generated. This pulse will not go true until at least 1/2 μs after the data is present at the outputs. Third, the inhibit timing cycle is initiated within 2 μs after the load and strobe inputs are generated and locks out the load and strobe inputs for the duration of the inhibit timing cycle. This insures that only one strobe is generated and no data is changed during the inhibit cycle.

If the input data disappears less than 1/2 μs after the completion of the delay cycle, it is possible that erroneous logic sequencing can take place. The symptoms are new data, but no strobe or no new data, but a strobe is generated.

If the output enable input is held false, no logic sequencing can take place and the chip remains locked up with the existing data statically available at the outputs and no strobes can be generated.

A programming option is available wherein a level strobe can be specified instead of the delayed strobe as described above. In this option, the level strobe goes true at the end of the delay cycle as does the delayed strobe, but is remains true as long as a valid data input signal is present. It is not affected by the inhibit timing cycle. The level strobe responds to the data input lines and is inhibited only by the Output Enable going false.

Debounce Circuits

The debounce circuits utilize a pulse train clock oscillator and shift registers. The input must remain in one state for 2 consecutive clock pulses before it will change the output to that state. The outputs follow the input, in that they are non-inverting.

OPTIONS

The following options are customer specified. (For format information, see Programming Format section).

Input Code

The input code M out of N (typically 2 out of 13) must be specified for each reprogramming of the coding mask.

Mode Select

The Mode Select lines bit pattern must be specified for each mode for each reprogramming of the coding mask. Each mode must be specified whether used or not.

Output Code

The Output Code must be specified for each input code and mode as above.

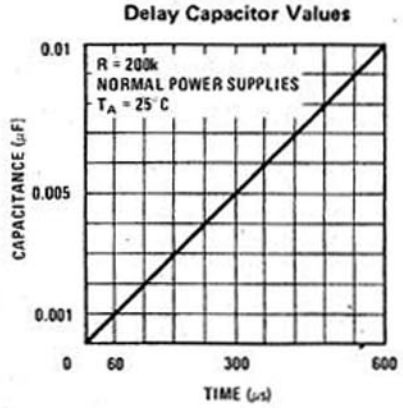
Strobe

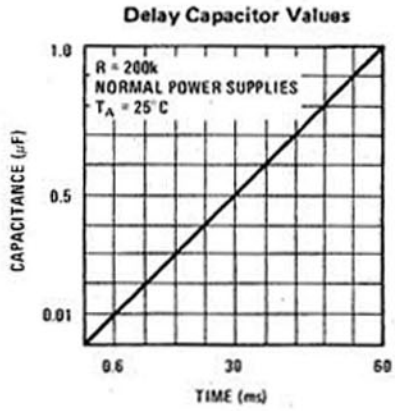
The Delayed Strobe is automatically selected unless the option for the level strobe is selected.

Input Resistors

Each of the 13 inputs and the 2 mode select inputs may have internal resistors (4.5 kΩ ±30%) connected to V_{SS}, V_{DD} or left open.

typical performance characteristics





timing diagram